Remarks

In the Office Action, Claim 5 was rejected as clearly anticipated under 35 U.S.C. §102(b) by Horden et al patent 5,812,860; and Claims 1-4 and 6-11 were rejected under 35 U.S.C. §103 as unpatentable over Horden. Claims 4, 5, and 7 are being canceled by this amendment. Claims 1-3, 6, and 8-11 remain in the application.

The Examiner rejected Claims 1-3 and 5-9 as unpatentable under 35 U.S.C. §103 over Horden. Claims 1, 2, 6, 8, 10, and 11 have been amended to overcome the rejection. Withdrawal of the rejection as to the remaining claims, as amended, is respectfully requested.

Applicant has invented an improved method and apparatus for reducing the power consumed by a computer processor. As applicants point out, it is desirable to use as little power as possible when operating a computer by reducing the frequency of operation of the processor and various other components associated with the processor to the minimum necessary to accomplish the operations being executed by the processor. As explained at page 2, line 22, through page 3, line 12, prior to the invention, this had been accomplished by one or more frequency generators, state machines or power management units, and power supplies al of which are external to and separate from the processor itself. Frequency generators which are external to the processor cause delays in crossing various interfaces, eliminated the ability to provide frequencies which may be changed in different ratios for different components, and generally slowed processing.

As will be seen by studying the Horden patent, this prior art apparatus and method is identical to what is disclosed in Horden (see Figure 1). Horden uses one or more external frequency generators 8, external power supplies 7 and voltage regulators 5, and external state machine 6.

The present invention improves on the prior art by providing a frequency generator on the same silicon chip as the processor. This eliminates the various interfaces which slow operation, allows direct control of the frequency by the processor itself, and facilitates the maintenance of a plurality of optimum frequencies for different components associated with the processor under control of the processor. None of these are possible utilizing prior art knowledge including that of Horden.

Horden does not suggest placing a frequency generator on a single chip with a processor. The Examiner states that it would be obvious to place a frequency generator on chip citing MPEP1244.04 V B.

In fact, the MPEP reference is directed to simply integrating elements onto a single chip where the integration is all that is accomplished. It does not relate to integrating elements on chip where an unobvious result is accomplished. In applicants' invention, integration makes possible furnishing individually selectable frequencies concurrently to different components of the processor and other functional components, a result which is not taught by the prior art including Horden and is not possible with the pior art teachings.

Applicants' claims include (or have been amended to include) language requiring that the frequency generator be on-chip with the processor and that the clock generator on the chip be capable of providing a plurality of

clock frequencies which can be individually selected concurrently. For example, Claim 1, as amended recites:

> A method for controlling the operating condition of a computer processor on a chip including a clock generator on the chip capable of providing a plurality of clock frequencies which can be individually selected concurrently comprising the steps of:
>
> determining a maximum allowable power consumption level from the operating condition of the processor,
>
> determining a maximum frequency which provides power not greater than the allowable power consumption level,
>
> determining a minimum voltage which allows operation at the maximum frequency determined, and
>
> dynamically changing the operating condition of the processor by changing one of the frequencies generated by the clock generator and the voltage to the maximum frequency and minimum voltage determined.

All of the other claims remaining include similar limitations.

The Office Action stated that applicants' arguments had been fully considered. However, the Examiner may wish to reconsider the statement of law expressed in finding those arguments are not persuasive. The Office Action appears to confuse the meanings of the words "suggest" and "explicitly state" in reaching this decision. This leads to the conclusion that no individual prior art need suggest the

combination which is applicants' invention. Instead, there seems to be some general aura of prior art which hovers in the background and of which all persons skilled in the art are aware whenever there would be a beneficial result. If this is true, then some portion of that prior art must suggest the combination; and it is up to the Examiner to provide this art to applicants for consideration. Otherwise, this legal conclusion is just another way of utilizing the hindsight gained from applicants' invention.

Since Horden (nor any other cited prior art) does not teach, disclose, or suggest in any manner the on-chip frequency generator which generates a plurality of frequencies concurrently for operating different components of a computer, the withdrawal of the rejection of Claims 1-3, 6, and 8-11, as amended, as obvious under 35 U.S.C. §103 is respectfully requested.

Since all claims now in the application appear to be allowable over the rejections included in the Office Action, the allowance of those claims, as amended, and the issuance of the application as a patent are respectfully requested.

Respectfully submitted,

5/7/02

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Version with markings to show changes made:

Please amend the claims as follows:

In the claims:

Cancel Claims 4, 5, and 7.

Please substitute the following claims for pending claims of the same number:

Claim 1 (twice amended). A method for controlling the operating condition of a computer processor on a chip including a clock generator on the chip capable of providing a plurality of clock frequencies which can be individually selected concurrently comprising the steps of:

determining a maximum allowable power consumption level from the operating condition of the processor,

determining a maximum frequency which provides power not greater than the allowable power consumption level,

determining a minimum voltage which allows operation at the maximum frequency determined, and

dynamically changing the operating condition of the processor by changing one of the frequencies[y] generated by the clock generator and the voltage to the maximum frequency and minimum voltage determined.

Claim 2 (amended). A computing device comprising:

a power supply furnishing selectable output voltages,

a clock frequency source,

a central processor including:

a processing unit for providing values indicative of operating conditions of the central processor, and

a clock frequency generator receiving a clock frequency from the clock frequency source and providing a one of a plurality of selectable output clock frequencies[y] to the processing unit; and

means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device.

Claim 6 (twice amended). A method for controlling the power used by a computer comprising the steps of:

utilizing control software to measure the operating characteristics of a central processor of the computer,

determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted, and

changing the operating characteristics of the central processor to a level commensurate with the operations being conducted in which:

the step of determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted comprising utilizing the control software to determine desirable voltages and frequencies for the operation of the central processor based on the measured operating characteristics, and

the step of changing the operating characteristics of the central processor to a level commensurate with the operations being conducted comprises providing signals:

for controlling voltages furnished by a programmable power supply to the central processor, [and]

for controlling frequencies furnished by the central processor to the central processor, and

providing signals for controlling frequencies furnished by the central processor to other functional units of the computer.

Claim 8 (amended). A computer comprising:

a power supply furnishing selectable output voltages,

a clock frequency source,

a bus,

system memory,

a central processor including:

a processing unit for providing values indicative of operating conditions of the central processor, and

a clock frequency generator receiving a clock frequency from the clock frequency source and providing a plurality of selectable output clock frequencies[y] to the processing unit; and

means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device including system memory.

Claim 10 (amended). A computing device as claimed in Claim 8 in which [the clock frequency generator provides a plurality of selectable output clock frequencies, and]

the means for detecting the values indicative of operating conditions of the central processor causes the clock frequency generator to generate frequencies which are selected for optimum operation of [a plurality of functional units of the computing device including] system memory.

Claim 11 (amended). A computing device as claimed in Claim 8 in which [the clock frequency generator provides a plurality of selectable output clock frequencies, and]

the means for detecting the values indicative of operating conditions of the central processor causes the clock frequency generator to generate

frequencies which are selected for optimum operation of [a plurality of functional units of the computing device] including the bus.